



Digital Darwinism

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Survival of the Fittest

- ✍ **Competition breeds innovation**
- ✍ **Successful innovation is bred from a strong knowledge base and established infrastructures**



Top 10 AMD Famous Quotes

10. *"They don't have enough FAB capacity!"* – 1994
9. *"AMD will never get the consumer market. Their competitors have too much brand equity!"* – 1995
8. *"AMD will never have 3rd party chip-sets specific for their CPUs!"* – 1996
7. *"AMD is selling the AMD K6 since it's pin-compatible. They will never establish a new bus infrastructure!"* – 1997
6. *"AMD simply doesn't have the FPU and nobody will support 3DNow!"* – 1997
5. *"They will never attain the MHz – their process sucks!!"* – 1998
4. *"EV6? What is EV6?!"* – 1999
3. *"They have too much FAB capacity!"* – 1999
2. *"DDR will never take off!"* – 1999
1. *"AMD never innovates..."* – Last Week



AMD Introduces Two New Pieces of Technology

GOAL: FASTER, MORE FUNCTIONAL TECHNOLOGIES

Innovation: AMD x86-64 technology

 Knowledge Base: Instruction sets, software, user experience

Innovation: AMD HyperTransport™ (previously codenamed “LDT”)

 Designed to move data inside a PC

 Designed to provide a high degree of scalability faster in a computer architecture

 Knowledge Base: X86 PC Platform, AMD comm. business



What Digital Darwinism Means to YOU

MIS/Users

- » Leverage your existing knowledge base and experience
- » Retain billions of dollars invested in current software, hardware and training
- » Low risk of introduction of new technologies into the enterprise

Developers

- » Leverage your existing tools, methodologies, and years of developed skills
- » Faster time-to-market for your products
- » Preserving your existing customer base



Observations on 64-bit Computing

Architecture

- ? New instruction sets require huge investment in training, development costs and tools
- ? Market needs a long, smooth transition to 64-bit applications

Performance


- ? Instruction sets don't address the major issues
 - » Control flow predictability
 - » Operation latency (especially memory latency)

**An ideal solution delivers industry leading performance
and seamlessly spans BOTH 32- and 64-bit applications**




The Innovative Approach: AMD's x86-64 Technology

 **Extends the x86 instruction set while maintaining compatibility with today's software**

 new operands, same operators

 same instruction lengths - no code bloat

 full 64-bit power for applications that need it

 Designed to run today's 32-bit OS's and applications with cutting-edge performance



The Innovative Approach: AMD's HyperTransport™ Technology

Compatible with today's Operative Systems

- ? PCI mechanism implemented
- ? Transparent to the user and to the applications

Straight forward approach

- ? Designed to provide a quantum leap in speed vs. competitive technologies
- ? Packet Bus in a PC designed to minimize conflicts, arbitration, bottlenecks and latency. Maximizes speed, scalability, design longevity.
- ? Great number of I/O devices in the market starting in 2nd half 2001



AMD's 8th Generation "Hammer" Processors



 **GOAL: SUSTAIN & INCREASE PERFORMANCE LEAD**

 **Innovation: Performance = Clock speed x architecture**

 Architectural performance innovations

 Pipeline supports aggressive clock speed scaling

 **Platform Knowledge Base: x86-64, DDR DRAM, AMD HyperTransport™ Technology**

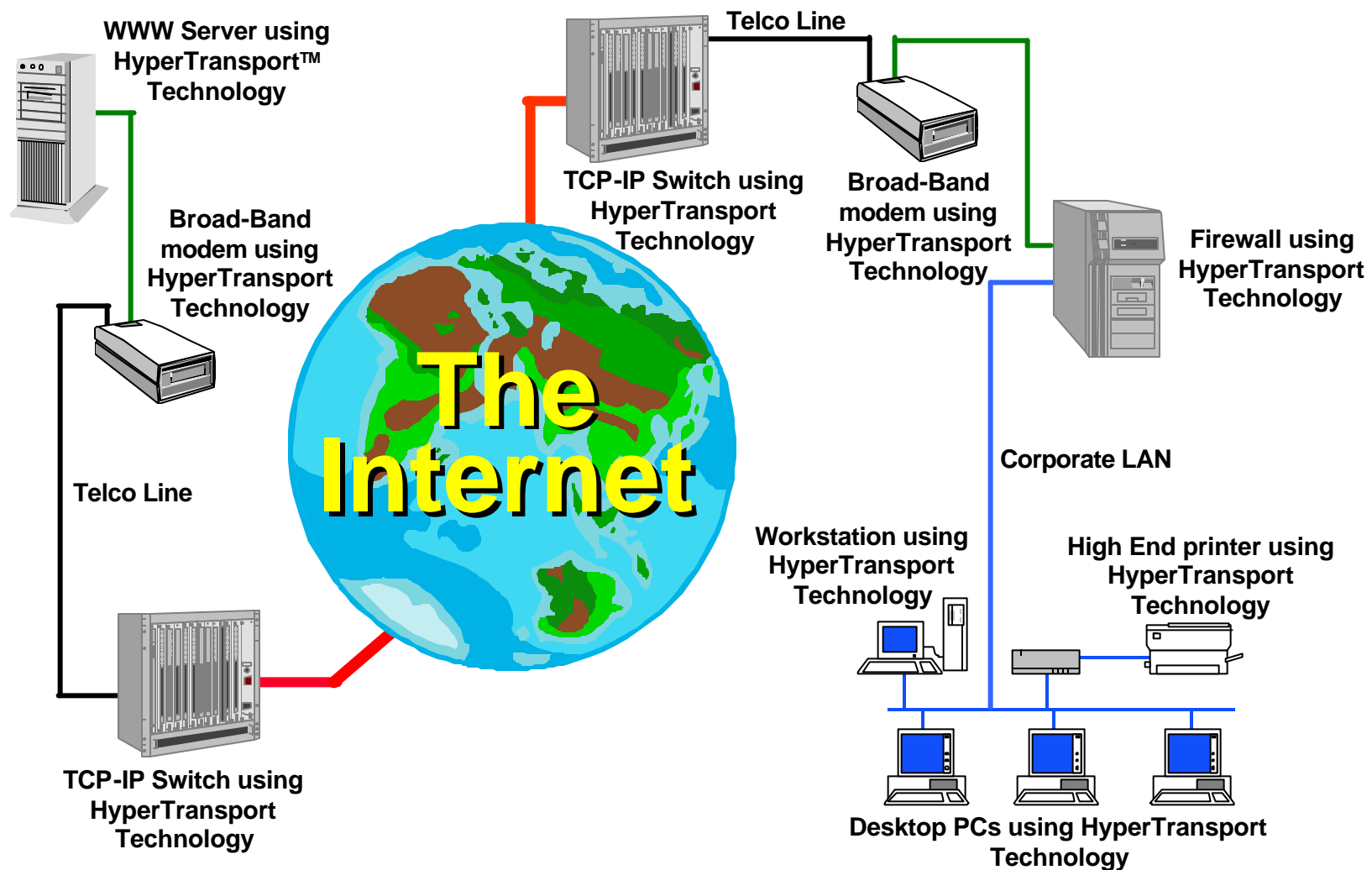


AMD HyperTransport™ Bus (formerly codenamed “LDT”)

- ✍ **Open standard for building high-bandwidth I/O subsystems to help address latency**
 - ✍ 1.6 Gbit/sec per data bit signaling
 - ✍ > 6 GBytes/s I/O subsystems: PCI-X, Gigabit Ethernet, InfiniBand, etc
- ✍ **Innovative new high-speed interconnect builds on existing work**
 - ✍ PCI device enumeration and setup methods
 - ✍ PnP header already defined
 - ✍ LVDS inspired signaling

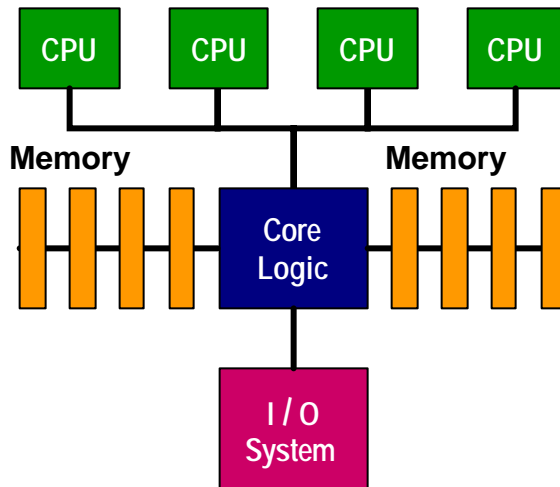


AMD HyperTransport™ For Internet Acceleration

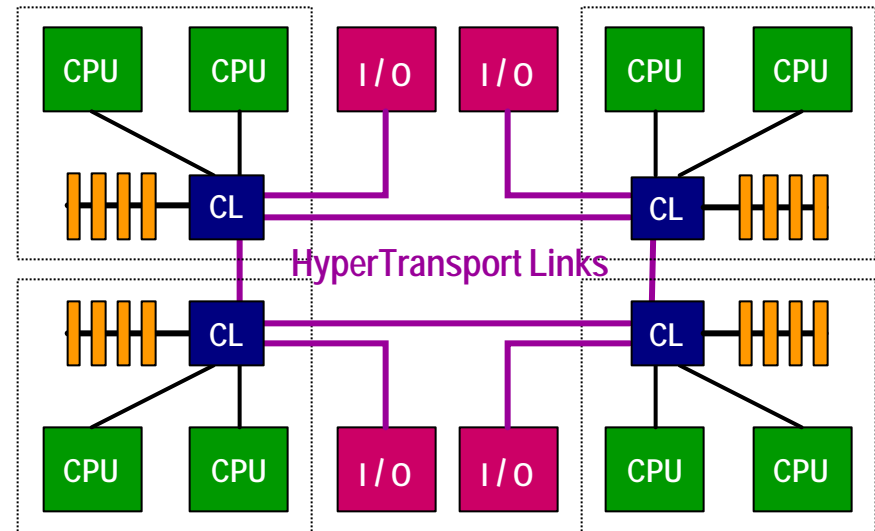


Highly Scalable Multiprocessing

Shared Bus Architecture



SMP HyperTransport Architecture



✂ Scalability limits

- ? Shared CPU buses force CPUs to share limited bandwidth
- ? More processors ✂ more memory bandwidth needed
- ? More IO bandwidth needed too

✂ SMP HyperTransport™ Architecture Improves Scaling

- ? HyperTransport designed to ease memory and I/O bandwidth scaling
- ? Coherent HyperTransport, an extension of HyperTransport



The Better Choice for Enterprise Computing

- ✍ **The most straightforward approach to 64-bit computing**
 - ? Not a major disruption, preserves existing instruction set
 - ? Familiar methodology for extending architecture

- ✍ **Seamless integration with existing environments**
 - ? Designed to introduce advantages of 64-bit while retaining existing software, tools, drivers, etc.
 - ? Leverages the knowledge base, toolchain, and billions of dollars invested in existing software
 - ? Maintains existing support and maintenance procedures



Summary

- ✍ **Successful innovations in the market will be built on established infrastructure**
- ✍ **Digital Darwinism will eliminate painful conversions**
- ✍ **AMD's Hammer family will emerge as a platform leader**
- ✍ **HyperTransport™ will be the leading chip-to-chip Bus in the Computation and Communication industry**

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